SIMULATION OF CNTFET DIGITAL CIRCUITS:
A VERILOG-A IMPLEMENTATION

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ABSTRACT
A Verilog-A compact model for Carbon NanoTube Field Effect Transistors (CNTFETs) has been implemented to study basic digital circuits. The model, based on the hypothesis of fully ballistic transport in a mesoscopic system between two non-reflective contacts, has been structured to allow an easy implementation in Verilog-A language and has been compared with experimental data, showing a good agreement between simulation and experimental results, particularly in the saturation region, where the relative error is practically negligible. Moreover the Verilog-A model has been utilized to design a digital NOT gate with complementary technology and a NAND gate, in which the quantum capacitance dependence on polarization voltages has been considered.

Keywords: Nanoelectronics, Carbon Nanotube Field Effect Transistors, Modelling, Quantum Effects, Circuit Simulation

1. INTRODUCTION
Prediction through modelling forms the basis of engineering design. The computational power at the fingertips of the professional engineer is increasing enormously and techniques for computer simulation are changing rapidly. Engineers need models which relate to their design area and are adaptable to new design concepts. They also need efficient and friendly ways of presenting, viewing and transmitting the data associated with their models.
A device model is considered a compact model because of the methods used to develop the equations and coefficients used for the electrical representation of the physical behaviour of a device. The word compact is used because these equations are simplified based upon several assumptions that are made when developing the model equations. On the other hand the availability of accurate, robust, and efficient compact models is critical to the successful utilization of any circuit simulation tool.
Nowadays the continuous reduction of electronic circuit size and power dissipation have been the ongoing theme in electronics industry. However as the feature size becomes smaller, scaling the silicon MOSFET becomes increasingly harder and this is mainly due to quantum mechanical tunneling of carriers through the thin gate oxide, to quantum mechanical tunneling of carriers from source to drain and from drain to body and to control of the density and location of dopant atoms in the channel and source/drain region to provide high on/off current ratio.
There are many solutions proposed to circumvent these limitations. Among them, Carbon Nano Tubes (CNTs) are currently considered as promising building blocks of a future nanoelectronic technology. In particular the Carbon NanoTube Field Effect Transistors (CNTFETs) are regarded as an important contending device to replace conventional silicon transistors [1]. The CNTFETs have molecular building block not coming from lithography and, along with these devices, molecular electronics must change the equation in our tool box. We drop out well known partial differential equation for charge diffusion and we use quantum mechanic to describe electrons, holes, atoms, molecules and photons [2]. In fact the research in the field of nanoelectronics is highly interdisciplinary, covering the domains of chemistry, material science, physics, and engineering with their methods and the extremely wide range of length and complexity scales. Advanced knowledge of such fields has necessarily to be combined. In addition, the complexity of quantum laws, which start playing a dominant role in nanoelectronics, makes attempts to treat complete devices (and even more so complete circuits) practically impossible, with approaches at the level of a full quantum description, so that at the cross-road of new materials and nanoelectronics only multiscale modeling approaches can progress knowledge sufficiently fast in the near future.
These new technologies and devices require the creation of accurate compact models, suited to the circuit design and easily translatable into a Hardware Description Language (HDL).
About modelling issues, most of the CNTFETs models available in literature are numerical and make use of self-consistency and therefore they cannot be directly implemented in modelling languages to design electronic circuits, such as SPICE, Verilog-A or VHDL-AMS. Moreover in the development of these new models we must faced the problem of their simulation in real circuits.
As a general rule, the modelling of these new devices implies the solution of a set of Partial Differential Equations (PDE). In this case the way to obtain correct results is to write a program, written ad hoc, for mathematical
computation software (like Octave, Matlab), which allows in short time to obtain current-voltage characteristics of the simple device.

However, when we must simulate real complex circuits, we require the help of graphical interfaces to acquire circuit schemes and to translate them in equations systems, which are typical tools of electronic simulations software. In particular, when the device behaviour can be expressed as a set of equations non involving PDE, i.e. using a compact model, it is possible to utilize some of the most useful tools available in electronic simulation software, having the component libraries and the graphic interface for the schematic drawing to obtain circuit netlist and circuit equations automatically. These both functions are the key point to reduce processing times, but, when circuits become complex, it is very difficult to solve and to check, one by one, a large system of integral-differential non linear coupled equations, using, for example, Octave or Matlab. For this reason an electronic simulation software requires that the device should be described in an hardware description language.

The most widely used language available nowadays is SPICE, or any of its evolution, with various graphical interfaces. Another language which has a solid implementation is Verilog-A, very interesting since it allows devices description in a syntax quite near to C programming language.

In [2-3] we have proposed a compact, semi-empirical model of CNTFET, in which we have introduced some improvements to allow an easy implementation in the SPICE simulator. In particular the model is based on the hypothesis of fully ballistic transport in a mesoscopic system between two non-reflective contacts. In this case, the drain current due to the electrons in a single sub-band can be evaluated by the Landauer formula and the total current is the sum of the contribution from the electrons in all the sub-bands which lie at least partially below the Fermi level of the source contact. Moreover, to avoid the resort to self-consistency, three parameters, depending on the nanotube diameter and the insulator capacitance, have been introduced and two coefficients, depending on the sub-bands minima, have been introduced to evaluate the charge in the channel.

The CNTFET equivalent circuit is similar to a common MOSFET one, in which flat band voltage has to be determined experimentally, resistances of the doped regions in series with the parasitic ones of the electrodes are commonly assumed equal to 25 KΩ (typical value of quantum resistance) and the quantum intrinsic capacitances have to be computed from the charge in the channel.

In this paper we have implemented our CNTFETs model in Verilog-A language to study basic digital circuits, obtaining a better implementation of capacitance model, because no limit has been introduced to sub-bands number.

The presentation is organized as follows. Section 2 gives a brief description of the proposed CNTFETs model. The Verilog-A implementation of the model is presented in Section 3, while the study of a digital NOT gate with complementary technology and a NAND gate with our Verilog-A code is given in section 4. The conclusions are described in Section 5.

2. MODEL DESCRIPTION

2.1 I-V model

The proposed model, developed for a n-type conventional CNTFETs [2-3], is based on the hypothesis of ballistic transport and makes reference to a work of A. Raychowdhury et al. [4] and on the following improvements introduced by F. Prégaldiny et al. [5-6] to solve some numerical problems of the original paper [4].

When a positive voltage is applied between drain-source (V_{DS} > 0 V), the hypothesis of ballistic transport allows to assert that the current is constant along the CNT and therefore it can be calculated at the beginning of the channel, near the source, at the maximum of conduction band, where electrons from the source take up energy levels related to states with positive wave number, while the electrons from the drain take up energy levels related to states with negative wave number.

When a positive voltage is applied between gate-source (V_{GS} > 0 V), the conduction band at the channel beginning decreases by qV_{CNT}, where V_{CNT} is the surface potential and q is the electron charge. With the hypothesis that each sub-band decreases by the same quantity along the whole channel length, the drain current for every single sub-band can be calculated using the Landauer formula [7]:

\[ I_{DSp} = \frac{4qkT}{h} \ln\left(1 + \exp\left(\frac{\xi_{Sp}}{kT}\right)\right) - \ln\left(1 + \exp\left(\frac{\xi_{Dp}}{kT}\right)\right) \]

(1)

where k is the Boltzmann constant, T is the absolute temperature, h is the Planck constant, p is the number of sub-bands, while \( \xi_{Sp} \) and \( \xi_{Dp} \) have the following expressions:

\[ \xi_{Sp} = \frac{qV_{CNT} - E_{CP}}{kT} \quad \text{and} \quad \xi_{Dp} = \frac{qV_{CNT} - E_{CP} - qV_{DS}}{kT} \]

(2)

being \( E_{CP} \) the sub-bands conduction minima.

Therefore the total drain current can be expressed as [7]:

\[ I_{DS} = \sum_{p=1}^{p} I_{DSp} \]
The surface potential, $V_{\text{CNT}}$, is evaluated by the following approximation:

$$V_{\text{CNT}} = \begin{cases} V_{\text{GS}} & \text{for } V_{\text{GS}} < \frac{E_{\text{C}}}{q} \\ V_{\text{GS}} - \alpha \left( V_{\text{GS}} - \frac{E_{\text{C}}}{q} \right) & \text{for } V_{\text{GS}} \geq \frac{E_{\text{C}}}{q} \end{cases}$$

(4)

where $E_{\text{C}}$ is the conduction band minima for the first sub-band.

The parameter $\alpha$ depends on the $V_{\text{DS}}$ voltage and has the following expression:

$$\alpha = \alpha_0 + \alpha_1 V_{\text{DS}} + \alpha_2 V_{\text{DS}}^2$$

(5)

where $\alpha_0$, $\alpha_1$, and $\alpha_2$ are functions of both CNTFET diameter and gate oxide capacitance $C_{\text{ox}}$, must be extracted from the experimental device characteristics [2-3].

### 2.2 C-V model

To determine the quantum capacitances $C_{\text{GS}}$ and $C_{\text{GD}}$, it is necessary to know the total channel charge $Q_{\text{CNT}}$, having the following expression:

$$Q_{\text{CNT}} = q \sum_p (n_{\text{Sp}} + n_{\text{Dp}})$$

(6)

where $n_{\text{Sp}}$ and $n_{\text{Dp}}$ are electron concentrations by the source and drain respectively in the $p$-th sub-band. Having:

$$N_0 = \frac{4kT}{3\pi a_0}$$

(7)

where $a_0$ is the carbon-carbon (C-C) bonding distance ($\approx 0.142$ nm) and $\gamma$ the C-C bonding energy ($\approx 3$ eV), the number of carrier $n_{ip}$ ($i = S$ or $D$), which increases almost linearly as $\xi_{ip}$ greater or equal than zero and falls off exponentially as $\xi_{ip}$ becomes negative, can be derived from the following relationship [4]:

$$n_{ip} = N_0 \begin{cases} A_p \exp \xi_{ip} & \text{for } \xi_{ip} < 0 \\ B_p \xi_{ip} + A_p & \text{for } \xi_{ip} \geq 0 \end{cases}$$

(8)

where the parameters $A_p$ and $B_p$, depending on $E_{Cp}$, for $E_{Cp} < 0.5$ eV, have the following empirical expressions [4]:

$$\begin{align*}
A_p &= -5.3E_{Cp}^2 + 10E_{Cp} + 1 \\
B_p &= 0.34E_{Cp} + 1
\end{align*}$$

(9)

Therefore the quantum capacitances $C_{\text{GD}}$ and $C_{\text{GS}}$ are given by:

$$\begin{align*}
C_{\text{GD}} &= q \sum_p \frac{\partial n_{\text{Dp}}}{\partial V_{\text{GS}}} = q \sum_p \frac{\partial n_{\text{Dp}}}{\partial \xi_{\text{Dp}}} \frac{\partial \xi_{\text{Dp}}}{\partial V_{\text{CNT}}} \frac{\partial V_{\text{CNT}}}{\partial V_{\text{GS}}} \\
C_{\text{GS}} &= q \sum_p \frac{\partial n_{\text{Sp}}}{\partial V_{\text{GS}}} = q \sum_p \frac{\partial n_{\text{Sp}}}{\partial \xi_{\text{Sp}}} \frac{\partial \xi_{\text{Sp}}}{\partial V_{\text{CNT}}} \frac{\partial V_{\text{CNT}}}{\partial V_{\text{GS}}}
\end{align*}$$

(10)

However $V_{\text{CNT}}(V_{\text{GS}})$ and its derivative are not continuous for $V_{\text{GS}} = \frac{E_{\text{Cp}}}{q}$.

This problem can be solved by replacing Eqn. (4) with the following relationship [5]:

$$V_{\text{CNT}} = V_{\text{GS}} - \frac{\alpha}{2} \left( V_{\text{GS}} - \frac{E_{\text{C}}}{q} \right) + \sqrt{\frac{\alpha}{2} \left( V_{\text{GS}} - \frac{E_{\text{C}}}{q} \right)^2 + 4\varepsilon^2}$$

(11)

in which a smoothing parameter $\varepsilon$, assumed equal to 0.05 V as in [5], has been introduced.
The difference between Eqn. (4) and Eqn. (11) is negligible when \( V_{GS} \) is outside the range \( \left[ \frac{E_C}{q} - 2\epsilon, \frac{E_C}{q} + 2\epsilon \right] \). Also \( n_{ip}(\xi_{ip}) \) is not continuous for \( \frac{V_{GS}}{E_C} = \frac{E_{Cp}}{q} \). In this case it is convenient for \( n_{ip}(\xi_{ip}) \) an equation similar to the interpolation function of the EKV MOSFET model [8]:

\[
n_{ip} = N_0 \times 1.2B_p \left\{ \ln \left[ 1 + \frac{A_p}{1.2B_p} \exp \left( \frac{\xi_{ip}}{0.96} \right) \right] \right\}^{0.96}
\]

The CNTFET equivalent circuit, shown in figure 1, is similar to a common MOSFET one and is characterized by the generator \( V_{FB} \), for accounting the flat band voltage, and the resistors \( R_D \) and \( R_S \), in which the parasitic effect due to the electrodes are also included. Moreover we have considered also the CNT quantum inductance, assumed constant and equal to \( 4 \text{ pH/nm} \), which we have splitted up into two inductances of \( 2 \text{ pH/nm} \), while the classical self-inductance, as it is known [9], can be ignored.

3. **VERILOG-A MODEL IMPLEMENTATION**

In our previous SPICE simulations [2-3], however, we have found several problems:

1) any voltage over \( 10^9 \text{ V} \) triggers an overflow error by SPICE and therefore all model expressions must be scaled to avoid overcoming this limit in any connection. Similar overflow errors could happen also for the currents, but we have evaded this problem, since all utilized model expressions have been represented by voltages;

2) the switching between the values of two elaborate expressions has presented a severe drawback, since, even if it is easy to write a selector block, the circuits, which represent the expressions, are always both active, slowing the simulation, and both could trigger errors even when their output is neglected. For example, when \( \ln[1+\exp(x)] \) must be computed, we could avoid overflow problems switching, for \( x > 20.7 \), to the formula \( 1+x \). However, as the branch using “exp” is also active, it could determine overflow when the input was larger than 20.7. In this case, on the branch using “exp” the input value should be limited, making the code size larger and larger;

3) the gate-drain and gate-source capacitances, depend on bias voltages, can be obtained either as integral of current or as derivative of voltage. In the first case we introduce integration errors because of very small values of currents and time steps, while, in the second case, we introduce noise coming from derivative calculation. In fact, as we have used the derivative methods, in order to suppress noise instabilities, we need time filtering of the capacitance values, using an external RC circuit;

4) ABM blocks are not simulated exactly. In SPICE any simple block in the circuit is represented by an equation and, at each time step, the complete system of equations is solved by numerical approximations. This implies that the output of any ABM block is not the exact result of block operator applied to input, even for the most simple operators;
5) the schematic used to simulate the CNTFET model was so large that we have decided to use the capacitances dependent only on the first band, which is the dominant component of capacitances at low voltages. Furthermore we have simplified the expression concerning the capacitance using some quite good approximations, as we have described in the previous section. Nevertheless, when we have used our model to design some electronic circuits involved more CNTFET’s [2-3], the processing times have been quite high (also up to one hour).

6) Debugging of formulae, expressed with schematics, has been very difficult.

The previous problems have led us to utilize Verilog-A language [10], which is a part of Verilog-AMS, a high level description language for Analog and Mixed Signal circuits. For model developers accustomed to working in a standard programming language such as C, the switch to Verilog-A syntax should be straightforward and painless. The language is relatively succinct and compact, and is well-suited to analog model development. Nowadays several academic and industrial model development groups use Verilog-A as a key part of their development methodology.

Verilog-A language has a syntax that recalls in many aspects that of C and, for the numerical expressions, it has a mathematical library very similar to that of C. However one of the main difference from C syntax is the “contribution operator” (\(<\+)\), which is used to accumulate currents or voltages. Moreover, in our case, an important element of Verilog-A syntax has been the presence of “parameter” which could be set at run time: in this way we set nanotube diameter, length, number of electronic bands (to be accounted for current) and the kind of doping.

For example, for doping, the instruction line is:

```
parameter real doping = +1 from [-1,+1] ; // +1 p-type, -1 n-type
```

This last parameter was used avoiding, in this way, to duplicate code for n-type and p-type CNTFET.

In our work we use Verilog-A to describe the CNTFET in the ADS environment, while the rest of circuit was drawn with standard ADS libraries. After compiling the Verilog-A source, during the simulation, ADS calls the Verilog-A program to obtain values for the circuitual equations.

This organization of the work has presented the following advantages:

1) the model source code is independent of the simulator and it can be used on any simulator which has a Verilog-A compiler and interface;

2) the values of the device voltages or currents are computed by expression which are calculated using the mathematical library with high precision and in a very short time;

3) since we have no more the model expressions split in a graph of several elemental analogue blocks as with ABM in SPICE, the number of equations to be solved at each simulation step is widely reduced with important gain in speed and precision of the simulation;

4) the mathematical computation works in standard double precision, overflow errors are those standard to double precision, and there is no need to rescale variables;

5) during the simulation it is possible to trace the behaviour of intermediate expression in the Verilog-A program as it was possible with SPICE, but in Verilog-A it is also possible to obtain code controlled messages and to dedicate more space to the debugging code;

6) the complexity of the code is tiny compared to the complexity of the schemes used to reproduce expression with ABM blocks in SPICE and this allows us to implement the complete model in all details. The code results more clear and well organized and the programming errors are widely reduced;

7) since the code is simple and fast, there is space to implement also some mathematical optimizations to enhance the numerical precision. In the model we have implemented several times expressions of the form \(\ln(1+\exp(x))\) which suffers of a progressive lost of precision for \(x < -13\), so we implemented the following code based on the Taylor approximation:

```verilog
if (x < -13)
begin
    ex = exp(x) ;
    f = ex*(1-ex/2) ;
end
else
    f = ln(1+exp(x)) ;
```

8) furthermore, in order to have a more robust code, we implement also checks on input parameters and intermediate values. For example, since we want to be sure that the diameter value is realistic and not a typographical error, we write:

```verilog
parameter real diameter = 2e-9 from (3e-9:1e-7) ; // [m]
```

9) the gate-drain and gate-source capacitances, controlled in voltage, are implemented only in a couple of lines of code:

```verilog
icgs = ddt(cgs*vgs) ;
icgd = ddt(cgd*vgd) ;
```

10) we obtain a speed gain up to 100 compared to our model on ABM SPICE library, since any simulation requests few seconds unlike the SPICE version, in which several minutes are necessary for simulation.
Figure 2 compares the $I_{DS} - V_{DS}$ characteristics (denoted by continuous lines) of numerical simulations with Verilog-A language and the experimental ones [11] (denoted by ●), in which we have assumed the same values for $V_{FB}$, CNT diameter, $R_D$ and $R_S$ reported in [11].

![Figure 2: Simulated $I_{DS} - V_{DS}$ characteristics (denoted by continuous lines) and experimental $I_{DS} - V_{DS}$ characteristics [11] (denoted by ●).](image)

Figure 3 shows the implementation of the gate-drain and gate-source capacitances in Verilog-A version in which we have assumed $V_{FB} = 0$ V, CNT diameter = 1.4 nm, $R_D = R_S = 0$ Ω, $C_{ox} = 3.8$ pF/cm and $\varepsilon = 0.05$ V.

![Figure 3: Simulations of $C_{gd}$ and $C_{gs}$ vs $V_{ds}$ for different values of $V_{gs}$ using our Verilog-A model.](image)

The implementation of the gate-drain and gate-source capacitances has been different in SPICE [2-3] and in Verilog-A version, because in SPICE only one band in the capacitance model has been considered in order to do not weigh down the software further, while in Verilog-A no limit has been introduced to sub-bands number. However these differences have no influence on static characteristics, which are practically the same [2-3].

### 4. DIGITAL CIRCUIT SIMULATIONS WITH VERILOG-A

We have used the proposed CNTFET model to study basic digital circuits with Verilog-A. In all simulations we have considered CNTFETs having a diameter of 1.42 nm, length of 100 nm and quantum capacitances depending on polarization voltages.

The first circuit is NOT gates in a four stage chain, as shown in figure 4, whose circuit data are shown in the figure. Each NOT is designed with 3 identical CNTFET, the upper two working as dynamic load while resistors represent parasitic elements. The further fourth NOT gate has been used only to load the third stage. Moreover, since the proposed model is similar to conventional MOSFET one, it can be employed to design circuits using the same architectures than the ones used in standard CMOS technology.

In order to demonstrate also this statement, the circuit of figure 4 is implemented using complementary circuits with a N-CNTFET and a P-CNTFET.
The logic levels are at $V_+ = 0.1$ V and $V_- = -0.1$ V, the chain has been excited with a 120 ps trapezoidal wave with rise and fall time of 10 ps.

Figure 5 shows the transient simulation of NOT gate with complementary CNTFET technology, obtained with Verilog-A.

The delay has been obtained comparing the output of the first and of the third stage and it is 18 ps for SPICE simulations [2-3] and 17 ps for Verilog-A.

Both simulations show bumps just at the beginning of transitions and this derives from the difference of capacitance model in two languages. In fact, in our Verilog-A implementation, the number of sub-bands $p$ has been defined as a parameter settable by the user, while in the SPICE code it has been considered $p$ equal to 1 in the capacitance model to do not weigh down the software further.

Moreover the whole Verilog-A code of the model requires about 100 lines, in which 50 lines are declaration statements and only three intrinsic parameters are necessary: diameter, doping (+1 for n-type, -1 for p-type) and $V_{FB}$.

At last, we have studied NAND gates in a five stage chain, as shown in figure 6.

Figure 7 shows the result of the transient simulation in Verilog-A, in which we have considered quantum capacitances, $C_{GD}$ and $C_{GS}$, depending on the polarization voltages and $R_D$ and $R_S$ equal to 25 kΩ.
Also in this case the different voltage levels in the time dependent simulations with SPICE [12] and with Verilog-A comes from the incomplete implementation of capacitance model in SPICE.

5. CONCLUSIONS

In this paper a Verilog-A compact model for CNTFETs has been implemented to study basic digital circuits. The model, already proposed by us [2-3], is based on the hypothesis of fully ballistic transport in a mesoscopic system between two non-reflective contacts. In this case, the drain current due to the electrons in a single sub-band can be evaluated by the Landauer formula and the total current is the sum of the contribution from the electrons in all the sub-bands which lie at least partially below the Fermi level of the source contact.

The CNTFET equivalent circuit is similar to a common MOSFET one. In Verilog-A it has been possible to obtain a better implementation of capacitance model, because no limit has been introduced to sub-bands number.

Finally the Verilog-A model has been utilized to study a digital NOT gate with complementary technology and a NAND gate, in which the quantum capacitance dependence on polarization voltages has been considered.

Although SPICE has still an huge importance in the electronic design, since a great number of commercial devices are described by SPICE models and major chip producer distribute their simulation libraries for SPICE, we think that Verilog-A is an useful tool to help circuit designers to devise these very new nascent architectures, although its diffusion is still very limited and most of its libraries are dedicated to RF.

6. REFERENCES