MODELLING AND IMPLEMENTATION
OF SUBTHRESHOLD CURRENTS IN SCHOTTKY BARRIER CNTFETs
FOR DIGITAL APPLICATIONS

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ABSTRACT

The aim of this paper is to model and characterize the current voltage characteristics of Schottky Barrier (SB) Carbon NanoTube Field Effect Transistors (SB-CNTFETs) below and above threshold, in order to evaluate the noise margin and output voltage swing, whose values are necessary in the design of digital circuits.

Keywords: Carbon Nanotube Field Effect Transistors, Modelling, SubThreshold Currents, Noise Margin, Digital Applications

1. INTRODUCTION

Carbon nanotubes offer an intriguing solution to the scaling of silicon electronics [1]. Single walled carbon nanotubes [2], with their high carrier mobility and their possible metallic or semiconducting properties can be used in many electronic applications, such as the channel of transistors and metal interconnects [3] [4].

This work is centered around carbon nanotube applications to field effect transistors (FETs). Many research groups are studying CNT current, growth, and structure; however, little at this time has been done related to circuit characteristics and models, which form the basis of engineering design.

There are two main types of carbon nanotube FETs differing by their current injection methods: Schottky barrier FETs [5] [6] [7], and doped CNTFETs, [1] [2].

In this paper we refer only to Schottky Barrier (SB) carbon nanotube FETs, in order to model and characterize the current voltage characteristics of these devices below and above threshold. In this way it is possible to evaluate the noise margin and output voltage swing, necessary to digital circuits design.

The presentation of the paper is organized as follows. Section 2 gives a brief description of the operation of SB-CNTFETs. The Matlab implementation of the I-V model is presented in Section 3, while the study of a digital NOT gate with complementary technology is given in section 4. The conclusions are described in Section 5.

2. SB CNTFETs

To understand the operation of a Schottky barrier CNTFET, it is necessary to examine the energy band diagram for the structure. At the intersection between the metal contacts and the semiconducting carbon nanotube, Schottky barriers are created. The energy band diagrams are shown in Fig. 1 [2].

The current in CNTFETs is from the tunneling of carriers through the Schottky barriers. The type of metal for the contacts is chosen so that its work function forces the metal Fermi Level to lie between the valance and conduction band of the CNT [2].

For short channels, the CNT channel can become ballistic and hence, the metal contact resistance and the Schottky barriers at the source and drain ends limit the current drive through the nanotube. Thus, a low contact resistance, such as that of Titanium, is desirable. Presently, the control of the metal contacts to carbon nanotubes is not consistent and the tunneling current levels between transistors can vary greatly.

When a negative voltage is applied between the drain and source, the band structure, of the CNT, is modulated to account for the drain to source voltage (Vds), as shown in Fig. 1.

Figure 1. Band diagrams for a SB-CNTFETs in the ‘off’ and ‘on’ states respectively.
When a small negative gate to source voltage is applied, CNTFET is in the subthreshold condition. With a negative gate voltage applied, the Schottky barrier width at the source is modulated, allowing for holes or electrons to tunnel through the valence band and pass to the drain. This condition is shown in Fig.1b. The thickness of the source Schottky barrier at the metal Fermi level decreases exponentially with an increasing gate to source voltage. Thus, the tunnel current through the Schottky barrier increases exponentially, inversely to the barrier thickness.

In Fig.2 the exponential current-voltage characteristics of the subthreshold condition is shown.

![Figure 2. a) Subthreshold band diagrams for SB-transistors; b) I-V characteristics in subthreshold condition.](image)

Moreover Id-Vgs characteristic does not differ greatly changing Vds because the drain voltage does not significantly control the source Schottky barrier. This exponential current relation can be seen in Fig. 3 [5], in which it is easy to see that the subthreshold characteristics do not vary largely with Vds and the subthreshold slope remains relatively constant with temperature.

![Figure 3. Experimental Id versus Vgs subthreshold characteristics for a p-type transistor, with a channel length of 300 nm and a gate oxide thickness of 20 nm (from [5]).](image)

The transistor threshold voltage, where the device acts similarly to an ‘on’ MOSFET, is reached when the metal source Fermi level is approximately even with the valence or conduction band of the CNT, in a p-channel or n-channel respectively. If the gate voltage continues to increase above this threshold, the Schottky barrier thickness at the source will remain constant and the current will not continue to increase exponentially. Above the threshold voltage, the current will only increase linearly with Vds.

Above the CNTFET threshold voltage, the I-V characteristics are very similar to a MOSFET’s I-V characteristics: the current increases linearly with Vds; and, when the barrier at the drain is completely eliminated, the FET current saturates.

The Id-Vds characteristics for a saturated SB-CNTFETs have a very little slope, unlike short channel MOSFETs.

### 3. Id-Vgs CHARACTERISTICS MODELLING OF SUBTHRESHOLD CNTFETs

The portable electronics industry, expanded intensely in the recent years, requires voltage supply scaling, so that the supply voltage is lower than the threshold voltage of a transistor. For these low power applications, such as hearing aids, trade performance for power savings, the transistor must operate in subthreshold regime.
An important metric in subthreshold design is the ratio of on- to off-current ($I_{on}/I_{off}$). This ratio characterizes the difference in current between a closed and open switch. The on-current in MOSFETs decreases exponentially as the supply voltage is lowered. The same happens in carbon nanotube transistors. However, compared to MOSFETs, the off-current in CNTFETs continues to decrease as the voltage across the FET from drain to source decreases.

Carbon nanotubes have a varying $I_{on}/I_{off}$ ratio, depending on the nanotube structure and properties [1] [4]. These very high current values in CNTs are due to their ballistic transport and their limited electron and hole scattering [3]. Therefore, CNTs have the ability to increase performance while adhering to lower power requirements in subthreshold circuits.

In this paragraph we describe the procedure to model the current in SB-CNTFETs, operating in the low voltage, subthreshold regime, in order to determine the functionality of future subthreshold CNTFETs in digital design.

In order to model the Id-Vgs characteristics, we have implemented a Matlab code, characterized by a minimum current at $V_{DS}/2$, threshold voltage and exponential subthreshold current. In particular the following equations allow to value the current for a n-channel transistor (for a p-channel transistor we have the same expressions with negative voltages values):

\[ V_{th} = c \left( \frac{D_t}{2} \right) + d \]  
\[ V_{min} = \frac{V_{ds}}{2} \]  
\[ I_{D0} = 6.96 \times 10^{-20} \times e^{(9.17D_t)} \]  
\[ I_{Dmin} = I_{D0} \times e^{(b_n|V_{ds}|)} \]  
\[ I_{Dchannel} = I_{Dmin} \times e^{(a_n|V_{gs}-V_{min}|)} \]

where $c$ is equal to -0.125*10^-9 V/m, $d$ is equal to 0.6625 V and $b_n$ is a constant depending on the process variations [5]. Moreover $a_n$ is a fitting parameter, dependent on gate oxide thickness ($t_{ox}$) and on CNT diameter ($D_t$).

In the proposed model we have assumed $E_{Fermi} = E_{CNTmidband\_gap}$ and therefore the p-channel current characteristics are equal to the n-channel I-V data.

The obtained Id-Vgs characteristics, for a n-channel and a p-channel CNTFETs, are shown in Fig. 4 and 5 respectively.

In Fig. 4 we have assumed $D_t = 1.3$ nm and $b_n = 16.1$ V^-1s, while in Fig. 5 $D_t = 2.5$ nm and $b_n = 14.1$ V^-1s.
The CNTFET subthreshold regime is verified between the two threshold voltage ($V_{th}$) points. These points have the same distance from the minimum voltage.

The distance from the minimum to the threshold is $\Delta V_{SUB} (V_{ds}) = V_{th} - V_{min}$.

In Fig.6 we have reported the experimental Id-Vgs characteristics obtained by Appenzeller et al. [5][7] and our simulated ones, for a CNT diameter equal to 1.3 nm (up) and 2.5 nm (down).
In order to compare our model with experimental results, in Tables 1a) and 1b) we have reported the numerical values of $V_{\text{min}}$, $I_{\text{Dmin}}$ and $V_{\text{th}}$ obtained in [5][7] and those obtained by our model, for two SB-CNTFETs having diameters 1.3 nm and 2.5 nm respectively.

<table>
<thead>
<tr>
<th>$V_{\text{ds}}$ [V]</th>
<th>$V_{\text{min}}$ [V]</th>
<th>$I_{\text{Dmin}}$ [A]</th>
<th>$V_{\text{th}}$ [V]</th>
<th>$n_s$ [V$^{-1}$]</th>
<th>$D_t$ [nm]</th>
</tr>
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<tr>
<td>0.1</td>
<td>0.05</td>
<td>1.19*10$^{-13}$</td>
<td>0.58</td>
<td>16.1</td>
<td>1.3</td>
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<td></td>
<td>0.05</td>
<td>1.11*10$^{-13}$</td>
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<tr>
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<td>0.15</td>
<td>2.83*10$^{-12}$</td>
<td>0.58</td>
<td>16.1</td>
<td>1.3</td>
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<td></td>
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<td>3.73*10$^{-12}$</td>
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<tr>
<td>0.5</td>
<td>0.25</td>
<td>7.71*10$^{-11}$</td>
<td>0.58</td>
<td>16.1</td>
<td>1.3</td>
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<tr>
<td></td>
<td>0.25</td>
<td>7.22*10$^{-11}$</td>
<td>0.6</td>
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</table>

Table 1a. Numerical values of $V_{\text{min}}$, $I_{\text{Dmin}}$ and $V_{\text{th}}$ obtained in [5][7] (blue) and those obtained with our model (red), for a SB-CNTFET having diameter equal to 1.3 nm.
Table 1b. Numerical values of $V_{\text{min}}$, $I_{\text{Dmin}}$, and $V_{\text{th}}$, obtained in [5][7] (blue) and those obtained with our model (red), for a SB-CNTFET having diameter equal to 2.5 nm.

From Fig. 6 and Tables 1a) and 1b), it is easy to seen a good agreement between the experimental and simulated $I_d$-$V_{\text{gs}}$ characteristics, with a negligible relative error, and this supports the validity of our approach. Moreover, the computation is instantly, or with processing times too short to be evaluated. To perform all the simulations we have used a common Windows-based PC, equipped with a Pentium IV CPU and main memory of 1 Gbyte.

4. DESIGN EXAMPLE: SB-CNTFET INVERTER
In order to validate our model, we have designed NOT gates, shown in Fig. 7. Moreover, since the proposed model is similar to conventional MOSFET one, it can be employed using the same architectures than the ones used in standard CMOS technology.

Fig. 8 shows the voltage-transfer characteristic (VTC) of NOT gate, in which we have highlighted three separate regions: low input, region of transition and high input.

To maximize contemporary both the noise margins (NM), we need to assume them equal to half of the maximum supply voltage.

Moreover the VTC depends on CNT diameter. In fact, the $I_{\text{off}}$ current of an n-FET, with diameter $\geq 2$ nm, is greater than the $I_{\text{on}}$ of a p-FET, and therefore, increasing the diameter, the $V_{\text{out}}$ voltage value, for which the gate assumes logical value 1, will slightly decrease.

For smaller diameters we have an opposite effect. Nevertheless the $I_{\text{on}}/I_{\text{off}}$ ratio is enough high and the increase of $I_{\text{off}}$ does not substantially change the VTC.
Fig. 9 shows the calculated maximum Voltage Swing for which the logical values are 1 (high) and 0 (low), for supply voltage $V_c = V_{DD}$ equal to 0.4 V and 0.6 V respectively, versus the CNT diameter.

From Fig. 9 we can assert that, for diameters greater than 2 nm and supply voltage equal to 0.6 V, the voltage swing decreases.

Intersecting the previous calculated Id-Vds characteristics of the pFET with those of the nFET (Fig. 7) for a same value of Vin, we may obtain Vin versus Vout, as shown in Fig. 10.
It is easy to see that VTC changes if $V_{DD}$ decreases to 0.4 V. Moreover, in both the graphs, for a diameter of 1.3 nm, $V_{out}$ considerably decreases, because of the existence of minimum current to $V_{gs} = V_{ds}/2$ for the CNTFETs.

In digital applications it is necessary to evaluate the differences ($V_{OH\_MIN} - V_{IL\_MIN}$) and ($V_{IL\_MAX} - V_{OL\_MAX}$), as shown in Fig. 8, which are respectively the noise margin to the logical level 1 ($NM_H$) and the noise margin to the logical level 0 ($NM_L$). The noise margin $NM$ is defined as the least among the two values of $NM_H$ and of $NM_L$.

In order to maximize $NM$, it would be desirable $V_{IL\_Max} = V_{IL\_MIN}$.

In Tables 2 and 3 we have reported the calculated NM values of CNTFET inverter, for a supply voltage $V_{DD}$ equal to 0.4 V and 0.6 V respectively, and for different CNT diameters.

| $V_{DD}$ [V] | D [nm] | $V_{OH\_MIN}$ | $V_{OH\_MIN}$ | $V_{OH\_MAX}$ | $V_{OH\_MAX}$ | $V_{IL\_MIN}$ | $V_{IL\_MIN}$ | $V_{IL\_MAX}$ | $NM_H$ | $NM_L$ | $NM_H$ | $NM_L$ | $NM_H$ | $NM_L$ | $NM_H$ | $NM_L$ | $NM_H$ | $NM_L$ | $NM_H$ | $NM_L$ |
| 0.4 | 1.3 | 0.38 | 0.38 | 0.01 | 0.02 | 0.21 | 0.19 | 0.17 | 0.17 | 0.18 | 0.17 | 0.17 | 0.17 | 0.17 | 0.17 | 0.17 |
| 0.4 | 1.9 | 0.38 | 0.35 | 0.01 | 0.05 | 0.21 | 0.19 | 0.17 | 0.14 | 0.18 | 0.14 | 0.14 | 0.17 | 0.14 |
| 0.4 | 2.5 | 0.37 | 0.30 | 0.02 | 0.10 | 0.21 | 0.19 | 0.16 | 0.09 | 0.17 | 0.09 | 0.16 | 0.09 |

*Table 2. Noise margin of the inverter ($V_{DD} = 0.4$ V).*
From the analysis of the obtained data reported in Tables 2 and 3, we can deduce that, varying the CNT diameter from 1.3 nm to 2.5 nm, the maximum noise margin is 0.1 V.

In particular, for both polarizations, the optimal condition, with regards to noise margin, is obtained for a CNT having a diameter equal to 1.3 nm. Instead, for CNT diameters of 1.9 nm and 2.5 nm, the noise margin reduces because the I-V characteristics are not monotonous. In this case it is convenient to take the points where the voltage \( V_{\text{OUT}} \) worsens, that is, where \( V_{\text{IN}} = 0 \) or \( V_{\text{IN}} = V_{\text{DD}} \).

5. CONCLUSIONS

In this paper we have proposed a procedure to model the current in SB-CNTFETs, operating in the low voltage, subthreshold condition, in order to determine the functionality of future subthreshold CNTFETs in digital design. In this way, through a design example of a SB-CNTFET inverter, it has been possible to evaluate the noise margin and output voltage swing, in order to determine the optimal working condition.

6. REFERENCES


