ELECTRICAL CHARACTERISTICS OF STRAINED DOUBLE GATE MOSFET

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ABSTRACT

In this paper electrical characteristics of Strained Double Gate Metal Oxide Semiconductor Field Effect Transistor (DG MOSFET) and that of Conventional Double Gate MOSFET were investigated. A quantum mechanical transport approach based on non-equilibrium Green’s function (NEGF) method in the framework of effective mass theory is employed in this analysis. We evaluate the variation of the threshold voltage, the subthreshold slope, ON state current when channel length decreases. It is shown that the strained DG MOSFET gives high performance transistor value of the scaled transconductance and ON current that are greater than conventional DG MOSFET. Furthermore, comparison of unity current gain frequency fT of the devices, which represents key metric for device applications, shows that the performance of strained DG MOSFET is better than the conventional DG MOSFET.

Keywords: Strain, DG MOSFET, NEGF, unity current gain frequency.

1. INTRODUCTION

As the MOSFET gate length enters the nanometer regime, short channel effects, such as Drain-Induced Barrier-Lowering (DIBL), become more and more significant, thus, various device concepts such as DG MOSFETs is becoming extensively attractive [1-2]. A major impetus for using these devices is the improved gate control and the reduction in short channel behavior for them. Conventional CMOS technology is facing greater challenges in terms of scaling due to reduced gate control, increased short-channel effects (SCEs) and high leakage currents [3]. Double gate structures on undoped SOI (Silicon on Insulator) are promising to overcome short channel effects (SCE) in nanometer-scaled MOSFET. In addition, these devices exhibit a good Ion/Ioff and present a channel with high conductivity[1]. DG MOSFETs have emerged as promising devices for nano-scale circuits due to their better scalability below 20 nm. Due to the presence of double gate, the effective gate control increases, reducing SCEs[4].

Improvement in the VLSI/ULSI circuit speed may be achieved by enhancement of the charging current of the device. This will be possible if new materials with higher carrier mobility are considered as replacement for conventional silicon or if novel methods are employed to enhance the carrier mobility such as applying strain in Si channel [5-7]. The use of strained Si/SiGe material promises the improvement of speed performance of CMOS devices.

In this paper we analyze Strained and conventional DG-MOSFET using a quantum mechanical transport approach based on non-equilibrium Green’s function method in the framework of effective mass theory [8-9], with assuming that channel length varies from 7nm to 20nm regime.

2. DEVICE STRUCTURES

2.1 Strained DG MOSFET

The strained DG MOSFET studied here is presented in Fig. 1. The channel of device is undoped, source and drain are highly doped (N_D= 10^20 cm^-3) and those are in the same length (L_S,D=6.5nm). Aluminum has been used as metal gate with lateral SiO2 spacers partially covering source and drain regions. In this study, body length (T_body) is assumed 4nm, the thickness of SiGe layer is 1nm, channel length (L_ch) varies from 7nm to 20nm and the oxide thickness(t_ox) is 1nm.
Figure 1. Strained DG MOSFET simulated in this paper. The channel of device is undoped, source and drain are highly doped ($N_D = 10^{20}$ cm$^{-3}$). Aluminum has been used as metal gate with lateral SiO2 spacers partially covering source and drain regions. $T_{body}$ is 4nm, the thickness of SiGe layer is 1 nm, $L_{ch}$ varies from 7 nm to 20 nm and $t_{ox}$ is 1nm.

2.2 Conventional DG MOSFET

The Conventional DG MOSFET studied in this work is shown in Fig. 2. The channel of device is intrinsic silicon, source and drain are highly doped ($N_D = 10^{20}$ cm$^{-3}$) and those are in the same length ($L_{S,D} = 6.5$ nm). Aluminum has been used as metal gate with lateral SiO2 spacers partially covering source and drain regions. In this study, body length ($T_{body}$) is assumed 4nm, channel length ($L_{ch}$) varies from 7 nm to 20 nm and the oxide thickness ($t_{ox}$) is 1nm.

Figure 2. Conventional DG MOSFET simulated in this paper. The channel of device is intrinsic silicon, source and drain are highly doped ($N_D = 10^{20}$ cm$^{-3}$). Aluminum has been used as metal gate with lateral SiO2 spacers partially covering source and drain regions. $T_{body}$ is 4nm, $L_{ch}$ varies from 7 nm to 20 nm and $t_{ox}$ is 1nm.

3. SIMULATION METHOD

In the nanometer regime, the wave-like behavior of Electron becomes significant, and the tunneling current should be considered. So the semiclassical transport equation is not suitable. In this paper we use a quantum mechanical approach based on non-equilibrium Green's function and employ uncoupled mode space (UMS) approach[9-10].

Here, the quantum confinement is in one dimension (along Y axis), the calculation of the quantum electron density relies upon a solution of a 1D Schrodinger equation solved for eigen state energies $E_{iv}(x)$ and wavefunctions $\Psi_{iv}(x,y)$ at each slice perpendicular to the X axis and for each electron valley $v[11]$:

$$-rac{\hbar^2}{2m^*(x,y)} \frac{\partial^2 \psi_{iv}}{\partial y^2} + E_C(x,y)\psi_{iv} = E_{iv}\psi_{iv}$$

(1)
Where \( m^x_y \) is a spatially dependent effective mass in \( Y \) direction for the \( v \)-th valley and \( E_c(x,y) \) is a conduction band edge. The conduction band of silicon is characterized by anisotropic effective masses \( ml \) and \( mt \), where \( ml \) and \( mt \) are the longitudinal and transverse effective masses, respectively.

In practice, due to strong quantum confinement, usually only a few of the lowest subbands are occupied and need to be included in the calculations. On the other hand, subbands are uncoupled and transport equation is a 1D equation. Transport is computed by NEGF formalism in 1D subbands within the mode space approach. The self-consistent loop starts with an initial guess for the potential. Then, Schrödinger equation is solved using this potential and the electron density are computed as follows\[11\]:

\[
n(x, y) = 2\frac{k_eT}{\pi\hbar^2} \sum_{\nu} \sqrt{m^x(x, y)m^y(x, y)} \sum_{m} |\psi_{\nu}^m(x, y)|^2 \ln \left[ 1 + \exp \left( \frac{E_{\nu} - E_F}{k_B T} \right) \right] 
\]

Then, this density is fed back into the Poisson solver for the self-consistent calculation. Once convergence is achieved, the current is computed as shown below\[9\]:

\[
I = \frac{q}{2\pi\hbar} \int_{-\infty}^{\infty} T(E) [f_{1D}(\mu_S - E) - f_{1D}(\mu_D - E)] dE
\]

4. RESULTS AND DISCUSSION

The tensile strained-Si layer causes the energy levels of four fold and two fold valleys to split and the energy levels of two fold valleys to be located lower than that of four folds\[8\]. The energy band model for relaxed SiGe and strained-Si is generated based on Ref. \[12\]. The material properties are summarized in table 1. Figure 3 represents the source - drain current as a function of gate voltages for Strained DG MOSFET when \( V_{gs} \) is equal to 0.5V and channel length varies from 7nm to 20nm.

Similar I-V characteristic for Conventional DG MOSFET has been shown in Figure 4. It can be seen that the reduction of the channel length results in shifting the characteristics to the left and it is clear that as the channel length become smaller than 15nm, the subthreshold current rises dramatically. Since the drain current depends on the channel length, the threshold voltage of the devices should also be channel length dependent.

Electrical characteristics for Strained and conventional DG MOSFET are summarized in table 1 and table 2. It shows that threshold voltage is proportional to \( L_{eq} \) for both devices.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Eq. used</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electron affinity</td>
<td>( X_{\text{Strained-Si}} = 4.05 + 0.58x )</td>
</tr>
<tr>
<td></td>
<td>( X_{\text{SiGe}} = 4.05 - 0.05x )</td>
</tr>
<tr>
<td>Band gap energy</td>
<td>( E_{g,\text{Strained-Si}} = 1.12 - x(0.31 + 0.53x) )</td>
</tr>
<tr>
<td></td>
<td>( E_{g,\text{SiGe}} = 1.12 - 0.42x )</td>
</tr>
<tr>
<td>Conduction band offset</td>
<td>( \Delta E_c = 0.63x )</td>
</tr>
<tr>
<td>Valance band offset</td>
<td>( \Delta E_v = x(0.74 - 0.53x) )</td>
</tr>
</tbody>
</table>
In table 2, ON current is given for strained DG MOSFET and in table 3 it has been given for conventional DG MOSFET. ON current is computed current when \( V_{DS} = 0.4 \) V and \( V_{GS} - V_{TH} = 0.3 \) V [13]. It is observed \( I_{ON} \) in the Strained structure is more than the other. Also, it can be seen the subthreshold slope and DIBL in the Strained structure is relatively smaller than those in the conventional structure.

**Table 2. Simulation Results for strained DG MOSFET.**

<table>
<thead>
<tr>
<th></th>
<th>( L_{ch}=7)nm</th>
<th>( L_{ch}=10)nm</th>
<th>( L_{ch}=15)nm</th>
<th>( L_{ch}=20)nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Threshold Voltage(V)</td>
<td>0.195</td>
<td>0.248</td>
<td>0.281</td>
<td>0.292</td>
</tr>
<tr>
<td>Subthreshold Slope(mV/dec)</td>
<td>93.4</td>
<td>74.9</td>
<td>65</td>
<td>62</td>
</tr>
<tr>
<td>DIBL</td>
<td>0.522</td>
<td>0.487</td>
<td>0.483</td>
<td>0.441</td>
</tr>
<tr>
<td>ON Current (A/\mu m)</td>
<td>( 1.57\times10^{-3} )</td>
<td>( 1.15\times10^{-3} )</td>
<td>( 1.06\times10^{-3} )</td>
<td>( 9.63\times10^{-4} )</td>
</tr>
</tbody>
</table>
Table 3. Simulation Results for conventional DG MOSFET.

<table>
<thead>
<tr>
<th></th>
<th>$L_{ch}=7\text{nm}$</th>
<th>$L_{ch}=10\text{nm}$</th>
<th>$L_{ch}=15\text{nm}$</th>
<th>$L_{ch}=20\text{nm}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Threshold Voltage(V)</td>
<td>0.242</td>
<td>0.302</td>
<td>0.328</td>
<td>0.341</td>
</tr>
<tr>
<td>Subthreshold Slope(mV/dec)</td>
<td>97.7</td>
<td>76</td>
<td>66</td>
<td>64</td>
</tr>
<tr>
<td>DIBL</td>
<td>0.579</td>
<td>0.521</td>
<td>0.501</td>
<td>0.496</td>
</tr>
<tr>
<td>ON Current (A/µm)</td>
<td>$6.75\times10^{-4}$</td>
<td>$4.55\times10^{-4}$</td>
<td>$3.44\times10^{-4}$</td>
<td>$3.2\times10^{-4}$</td>
</tr>
</tbody>
</table>

Figure 5 shows the variations of drain current with drain voltage at $V_{GS}-V_{TH}=0.3\text{V}$ for $L_{ch}=7\text{nm}$. The drain current in the strained DG MOSFET is larger than the drain current for other structure.

Figure 6 shows simulated transconductance characteristics at the drain bias of 0.4 V of strained and conventional DG MOSFET with the channel length of 7 nm. It indicates that the transconductance of strained structure is enhanced at high gate drive, compared with that of conventional structure. This enhancement in transconductance of strained DG MOSFET is due to the electron velocity improvement.

![Graph showing drain current versus drain voltage](image1)

*Figure 5. Drain current versus drain voltage strained and conventional DG MOSFET at $L_{ch}=7\text{nm}$, when $V_{GS}-V_{TH}=0.3\text{V}$.**

![Graph showing transconductance](image2)

*Figure 6. Transconductance for strain and conventional DG MOSFET versus $V_{GS}-V_{TH}$ when $L_{ch}=7\text{nm}$ and $V_{DS}=0.4V$.**

The gate-source capacitance is series combination of the oxide and quantum capacitance as below[15]:

$$C_{GS} = \left[C_{OX}^{-1} + C_{Q}^{-1}\right]^{-1}$$  \hspace{1cm} (7)

$C_{OX}$ is classical capacitance and can be analytically obtained as[16]
where $\varepsilon_r$ is the oxide dielectric constant, $\varepsilon_0$ is the permittivity of vacuum, $t_{OX}$ is the oxide thickness and $T_{body}$ is diameter of body. Quantum capacitance can be defined as \[ C_0 = q^2 \frac{\partial n}{\partial E_{FS}} \] (9)

Figure 7 shows the variation of the gate capacitance for strained and conventional DG MOSFETs as a function of $V_{GS} - V_{TH}$ when $L_{ch} = 7$ nm. A lower capacitance is obtained for the strained structure. In Figure 7, we can see the intrinsic unity current gain frequency which is calculated from $f_T = g_{m}/2\pi C_g$. The unity current gain frequency $f_T$ in strained DG MOSFET is higher than that in conventional structure because of high transconductance and low capacitance in strained device (Figure 8).

\[
C_{OX} = \frac{2\pi \varepsilon_r \varepsilon_0}{L_n \ln \left( \frac{2T_{OX} + T_{body}}{T_{body}} \right)} = 550 \text{ pF} \text{nm}^{-1}
\] (8)

5. CONCLUSION
In this paper, we have analyzed a strained channel DG MOSFET for higher speed CMOS circuits. We employed quantum mechanical transport approach based on non-equilibrium Green’s function method in the effective mass
approximation. Von Neumann boundary condition was used in the source/drain and Dirichlet boundary condition for the gate contact. The electrical characteristics for this structure have been investigated in detail for different channel length. It was revealed that the drain current for the strained channel DG MOSFET was improved when compared to the conventional DG MOSFET. Strained DG MOSFET presents lower DIBL effect, lower sub-threshold slope and higher ON current.

The gate capacitance and transconductance of the strained DG MOSFET increased which resulted in improved unity current gain frequency in comparison with conventional DG MOSFET. Consequently, strained device is expected to be a promising transistor for high-frequency applications in ultra small scales.

6. REFERENCE


