ELECTRONIC PREVENTION OF ‘LOW-VOLTAGE-LOAD-DISCONECT-CYCLING’ IN BATTERY DRIVEN SYSTEMS

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ABSTRACT
Electronic comparator switching of battery load at a preset dept-of-discharge (DoD) has been highlighted. Use of NAND gates flip-flop circuit to prevent load voltage oscillation at the DoD is discussed. A precision battery load switching circuit comprising a comparator and a flip-flop has been designed, prepared, tested and results presented.

Keywords: Dept-of-discharge, Battery load-cycling, Comparators, Flip-Flop.

1. INTRODUCTION
One wrong use that can destroy a lead-Acid battery is to discharge it below its manufacturers specified discharge voltage limit (depth-of-discharge (DoD)), and leave it at such low voltage for a few hours. This situation results from the irreversible hardening of the discharge generated lead sulphate (PbSO₄) on both the positive and negative plates of the battery. To avoid this, all battery usage systems should be incorporated with discharge monitor/cut-out systems. These systems are designed in accordance with the specific battery discharge capacity. Battery manufactures rate discharge capacity to a specified cut-off voltage which corresponds to 100% depth of discharge for the battery. For lead–Acid batteries this cut-off voltage is typically 10.5 volts for a nominal 12 volt battery (1.75 volts per cell) [1]. When on load, the terminal voltage of the battery is less than its Open Circuit Voltage (OPV). When open-circuited at its DoD, the battery attempts a recovery to its OPV. A monitoring circuit sees a voltage above its preset low-voltage-disconnect set point (LVD). If the voltage span between the LVD and the load reconnect voltage (LRV) is small, the system experiences a cycling on and off rapidly at the low-battery-state-of-charge, possibly damaging the load or the system controller. In some systems, the common solution has been the use of integrated comparators and other circuits in integrated charge/discharge controllers. Typical examples are TDA7278 SGS Thomson microelectronics controller, Silvertel AG102 Deep discharge protection integrated circuit and MAX 791 microprocessor supervisory integrated circuit. Such “deep discharge” protection circuits switch off the load when the battery voltage drops to ~9.8V and prevents it from being switched back until the terminal voltage is raised above ~12.5V [2]. Unfortunately, this expansion of voltage span between the LVD and LRV prevents reload of the battery at voltages within this range. This sort of situation could arise in a solar PV system open circuited during the night use hours but which does not receive sufficient sunlight during the next day to charge the battery to its extended LRV. This process reduces the battery’s availability - the probability that the battery will be functioning correctly at any given time.[3].

This paper reports the use of a combination of a comparator and flip-flop in preventing this undesirable and potentially harmful oscillation as well as increasing the battery’s availability. The method exploits the latching property of an R-S flip-flop. The simple but effective circuit may find application in PV array systems and Power Inverter designs. In Nigeria, the recent widespread deployment of stand-alone solar street lighting systems will find this circuit helpful in prolonging the useful lifetime of the deployed batteries.

2. CIRCUIT DESIGN
2.1 Introduction: The project’s circuit diagram prepared with ‘Proteus Labcenter Electronics Intelligent Schematic Input system (ISIS)’ is presented in figure 1. It comprises a comparator and flip-flop circuits both driving control relays. In open loop configuration, the output of an operational amplifier is driven to positive saturation if its inverting input is a few hundred microvolts less than its non inverting input [4]. If a battery voltage is therefore connected to its inverting terminal and a reference voltage placed at its non-inverting terminal, when the battery voltage goes below the reference voltage, the operational amplifier (op.amp), should positively saturate. In the circuit, the op.amp, comparator at its first tripping drives a relay that applies a set (S) voltage to the S/R flip–flop. The flip-flop latches and its output drives a second relay that open circuits the battery load. The latching prevents the possibility of load voltage cycling.
2.2 Comparator:- The circuit will be driven by a 12V battery. At a DoD of 10.5V, the circuit should remain stable. Therefore a voltage regulator of 8V output was selected. This determined the relays to be of 6V coil type. The comparator consists of op. amp U2 configured as a precision under-voltage switch [4]. Zener diode D1, Resistors R1, RV1 and R2 combine to provide the reference voltage of 5V to the op. amp non-inverting input. D1 is a 500mW, 5.6V Zener. Operated at a safe power dissipation of 300mW, its current at 8V applied is 0.04A. Combining this value with its Vz of 5.6V gives R1 as 64Ω. The reference 5V is picked from the 5.6V Zener voltage across the RV1, 10KΩ variable resistor and R2. The direct battery voltage is connected to R3. R1 and R4 form a voltage divider to present the trip point voltage to the comparator inverting input. R4 is determined by equation 1 [5].

\[ R_3 = V_{\text{trip}} \times 2K\Omega - 10K\Omega \]  

(1).

For the specified 10.5V DoD, Eqn.1 gives R3 as 11KΩ. The output of the op. amp is coupled to a relay driving common emitter amplifier in such a way that the transistor is cut-off when the op. amp is negatively saturated and driven fully “ON” at positive saturation. The 6V coil miniature pcb relay at 8V exhibited a 10mA pull-in current with 118Ω resistor in series with the coil. Combined with its 106Ω dc coil resistance gives 36mA current at 8V. This minimum current will be supplied by the transistor collector. The transistor employed is a general purpose low wattage BC108, of the following specifications:- VCEmax. 80V, ICmax. 0.1A, Pmax. 0.5W [6]. Its current gain HFE was measured to be 260. Resistors R5 and RV2 set the base current at 40uA with the RV2 wiper approximately centered.

2.3 Flip–Flop circuit:- Regulator U2 provides 5V for the TTL logic gates obtained from integrated Quad 2-input NAND gates 74LS7400. The flip-flop along with Resistors R6, R8 pull-up resistors and reset switch J1 constitute a Contact Bounce Eliminator [7]. R7, RV1 and Q2 are equivalent to R, RV2 and Q1, respectively. To test the circuit, a 400W, 12VDC, 220V modified sinewave output voltage inverter was prepared and utilized. In order to ensure stability of voltage for the inverter oscillator and control circuits during the battery voltage drops, a 12V to 24V voltage doubler circuit was prepared and inserted between the battery and the control circuits. The 24V was further stabilized and reduced to 12V and 5V through the use of integrated voltage regulators LM 7812 and LM 7805.

While driving a 200W incandescent bulb, the inverter output waveform was monitored and recorded by a Velleman PCS100/8031 PC oscilloscope. The final stage of the tests involved channeling the power supply of the SG3524 inverter oscillator circuit through the two output relays of the comparator and comparator/flip-flop. The resulting voltage waveforms close to the Battery DoD were again recorded.

3. RESULTS AND DISCUSSIONS

Figure 2 shows a stepped down 220/24V modified sinewave output from the test inverter. The measured frequency was 73.5Hz.
Figure 3 shows the fluctuation those results from the comparator alone while attempting to switch off the system at the preset depth of discharge. The potentially dangerous oscillation is evident in the plot. This condition was eliminated when the Inverter oscillator drive-circuit was connected through the comparator/flip-flop output relay.

4. CONCLUSIONS
The prevention of battery/load oscillation as the battery discharges close to its lowest allowable limit is very important. This is because the prevention protects the battery’s cells and load equipment. The simple but effective circuit developed in this project will serve in achieving this target especially as it relates to all variants of lead-acid batteries.

5. REFERENCES