A COMPARATIVE ANALYSIS OF IMPACT OF TEMPERATURE VARIATION ON CNTFET DEVICE CHARACTERISTICS

Roberto Marani[1] and Anna Gina Perri[2]*

[1] National Research Council of Italy (CNR), Institute of Intelligent Industrial Technologies and Systems for Advanced Manufacturing (STIIMA), Bari, 70125, Italy
[2] Department of Electrical and Information Engineering, Polytechnic University of Bari, 70125, Italy
[3] The University of ABC, City, Country
[4] The University of ABC, City, Country
*Corresponding Author: annagina.perri@poliba.it

ABSTRACT

This paper presents a comparative analysis of impact of temperature variation on I-V characteristics in two CNTFET models proposed in literature in order to identify the one more easily implementable in simulation software for electronic circuit design. At first we consider a compact, semi-empirical model, already proposed by us, performing I-V characteristic simulations at different temperatures. Our results are compared with those obtained with the numerical FETToy model, online available, obtaining I-V characteristics comparable, but with CPU calculation times lower.

Keywords: *Nanodevices, CNTFET, I-V characteristics, Temperature Effects, Verilog-A, Computer Aided Design (CAD).*

1. INTRODUCTION

Nowadays the scaling operation of silicon devices is saturated since these devices cannot be more shrunk without degrading their performances for the arising of some phenomena like tunnel effects [1] or the perforation of the gate oxide also for voltages relatively low.

The previous problems can be overcome by resorting to other new devices, such as Carbon NanoTube Field Effect Transistors (CNTFETs) [2], in which, as it is known, the channel is formed by Carbon NanoTubes (CNTs) instead of silicon.

In literature various CNTFETs models have been proposed.

In [3-9] we have already proposed a compact, semi-empirical model of CNTFET, in which we introduced some improvements to allow an easy implementation both in SPICE, using ABM library, and in Verilog-A. Then our model has been implemented in [10-13] to carry out static and dynamic analysis of digital gates.

In this paper, we present a comparison of temperature dependence of I-V characteristics in two CNTFETs models proposed in the literature in order to identify the one more easily implementable in simulation software for CAD.

At first we consider a compact, semi-empirical model, already proposed by us [6-9], performing I-V characteristic simulations at different temperatures. Our results are compared with those obtained with a numerical model, online available, proposed by NanoHub in FETToy tool [14].

The presentation is organized as follows. Section 2 gives a brief description of the examined DC models, with reference to Equations on which the CNTFET models are based. The discussion of obtained results, together with the description of the setup-work used during the simulations, is given in Section 3. The conclusions and future developments are given in Section 4.

2. A BRIEF REVIEW OF THE TWO EXAMINES MODELS

An exhaustive description of our DC model is in [2-3], and therefore we recommend to the reader to see these references.

In this Section, we just describe the main equations on which our I-V model is based.

The total drain current I_{DS} in our model has been expressed using the Landauer formula [15]:

$$I_{DS} = \frac{4qkT}{h} \sum_{p} \left[\ln\left(1 + \exp \xi_{Sp}\right) - \ln\left(1 + \exp \xi_{Dp}\right) \right] \qquad (1)$$

where k is the Boltzmann constant, T is the absolute temperature, h is the Planck constant, p is the number of sub-bands, while ξ_{Sp} and ξ_{Dp} have the following expressions [3]:

$$\xi_{Sp} = \frac{qV_{CNT} - E_{Cp}}{kT} \quad \text{and} \quad \xi_{Dp} = \frac{qV_{CNT} - E_{Cp} - qV_{DS}}{kT} \tag{2}$$

being E_{Cp} the sub-bands conduction minima, V_{DS} the drain-source voltage and V_{CNT} the surface potential.
In [3] we have proposed, in order to evaluate V_{CNT}, the following approximation:

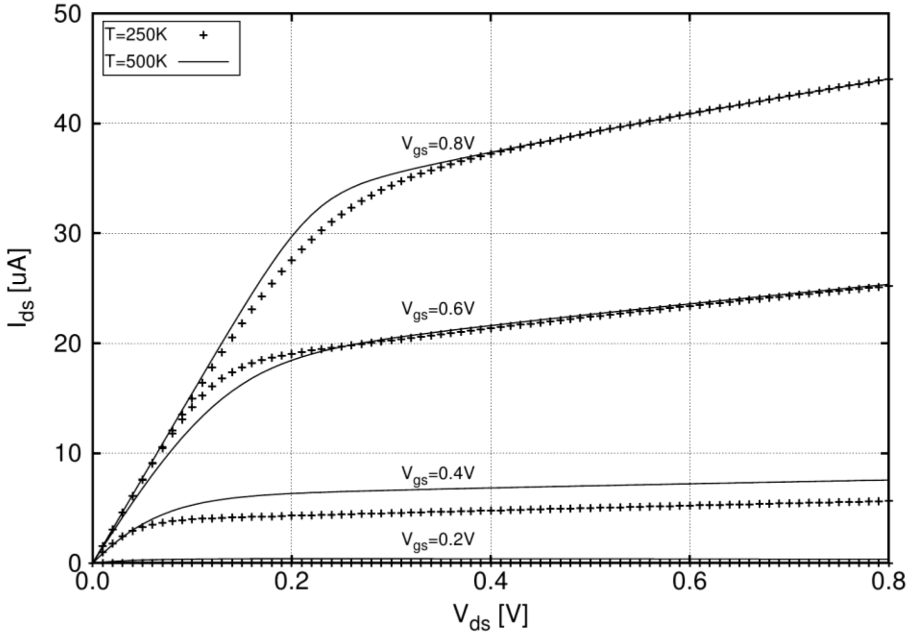
$$V_{CNT} = \begin{cases} V_{GS} & \text{for } V_{GS} < \dfrac{E_C}{q} \\ V_{GS} - \alpha\left(V_{GS} - \dfrac{E_C}{q}\right) & \text{for } V_{GS} \geq \dfrac{E_C}{q} \end{cases} \tag{3}$$

where E_C is the conduction band minimum for the first sub-band and α is a parameter depending on V_{DS} voltage, CNTFET diameter and gate oxide capacitance C_{ox} [3].
In the simulations, described in Section 3, our model has been translated in the programming language Verilog-A and then implemented on the simulator Advanced Design System (ADS).

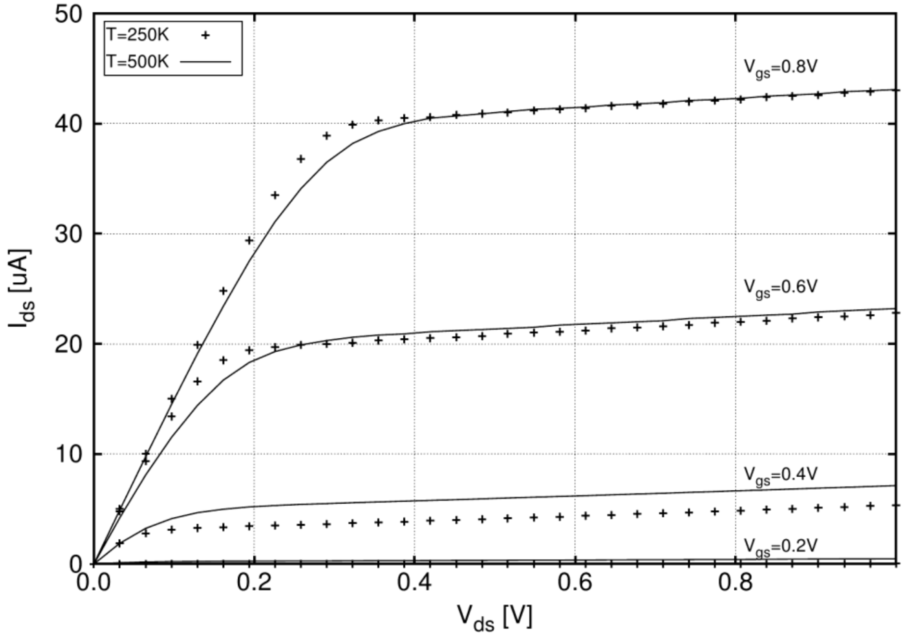
The model implemented in FETToy [14] is a purely numerical model. It is based on the non-equilibrium Green's function (NEGF) formalism, which solves the Schrödinger and Poisson equations under non-equilibrium conditions. The band structure of CNT has been calculated by the tight-binding method [16]. In particular FETToy simulator consists of a set of Matlab scripts that calculate the ballistic I-V characteristics for a conventional MOSFETs, Nanowire MOSFETs and Carbon NanoTube MOSFETs. Only the lowest subband is considered, but it is readily modifiable to include multiple subbands.
The underlying theory is described in detail in [16].

3. DISCUSSION OF SIMULATION RESULTS

We referred to the CNTFETs features reported in [17] to perform simulations with models described above.
The device has a zig-zag (19,0) CNT structure with approximately 1.5 nm radius which is embedded in cylindrical gate insulator of HfO_2 with the thickness and dielectric constant (k) of 2 nm and 16, respectively. The length of source and drain regions is equal to 20 nm. The channel is intrinsic and its length is 20 nm. There is no overlap between the source (drain) and gate regions.
The simulations are performed at the temperature of 250 K and 500 K in Agilent Technologies CAD ambient, Advanced Design System (ADS). In order to simulate with ADS, it has been necessary to develop a new component of the Design Kit, which was added to the model, written in Verilog language.
The results obtained from simulations, including those performed with FETToy, have been exported to a Matlab script. The graphs of this article are elaborated using Matlab.
Fig. 1 shows the I-V output characteristics of the two considered models, at various temperatures.
It can be observed from Fig. 1 that for low gate source voltages, at temperature of 500 K, the drain current I_{DS} is higher than that at 250 K. In spite of this, as V_{GS} increases at low drain source voltages, I_{DS} at 500 K is less than that at 250 K.
In the saturation region, by increasing V_{GS}, the drain current difference between high and low temperature reduces. It is evident from Figures 1 (a-b) that the drain current in the saturation region and V_{GS} = 0.8 V for 250 K and 500 K are approximately equal. This claim appears to be less verified for the FETToy model for V_{GS} = 0.6 V (Fig. 1 (b)).



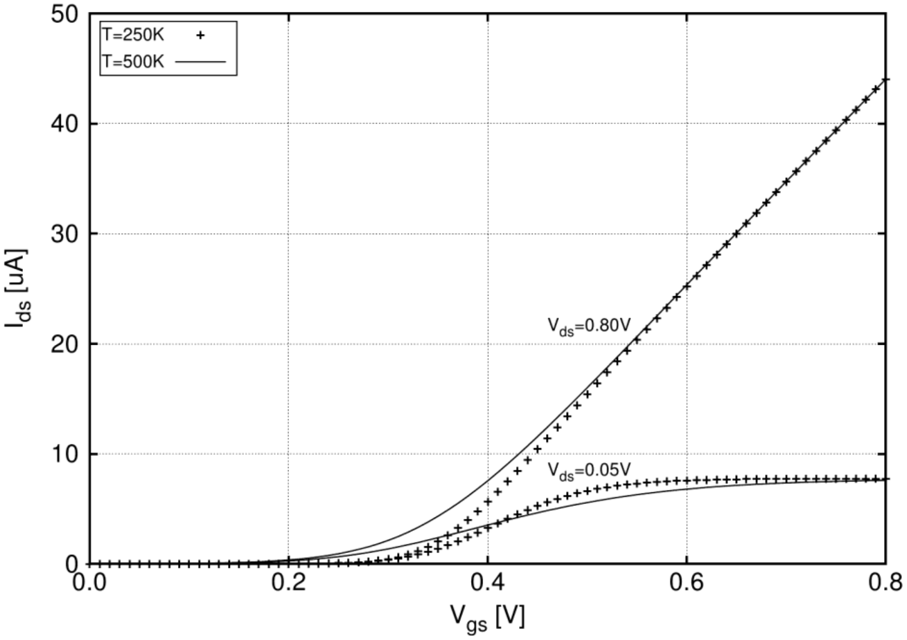
(a)



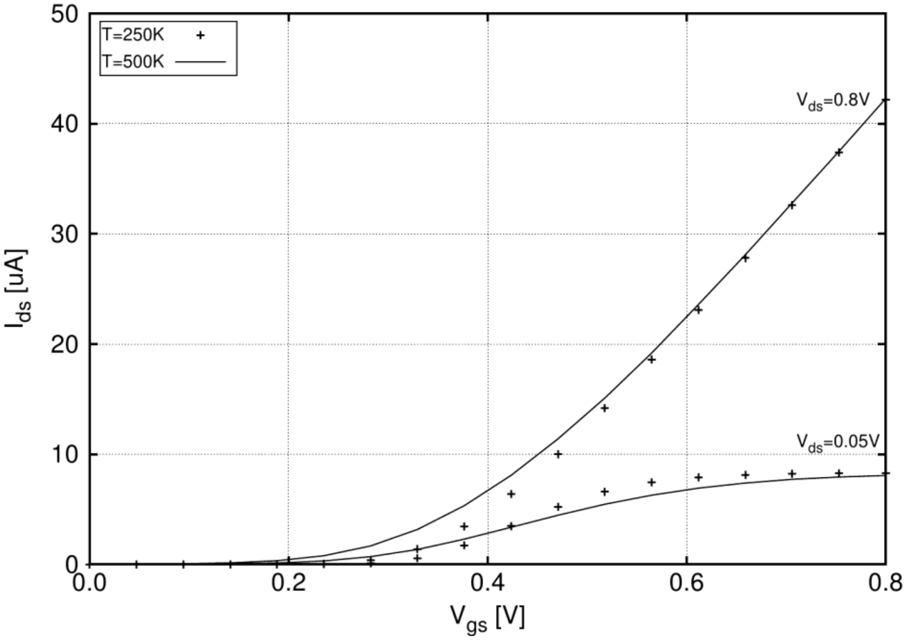
(b)

Figure 1. I_{DS} versus V_{DS} at different temperatures and different V_{GS} for:proposed model (a); FETToy model (b).

Similarly, Fig. 2 shows the trans-characteristics of the device, obtained by the considered two models.



(a)

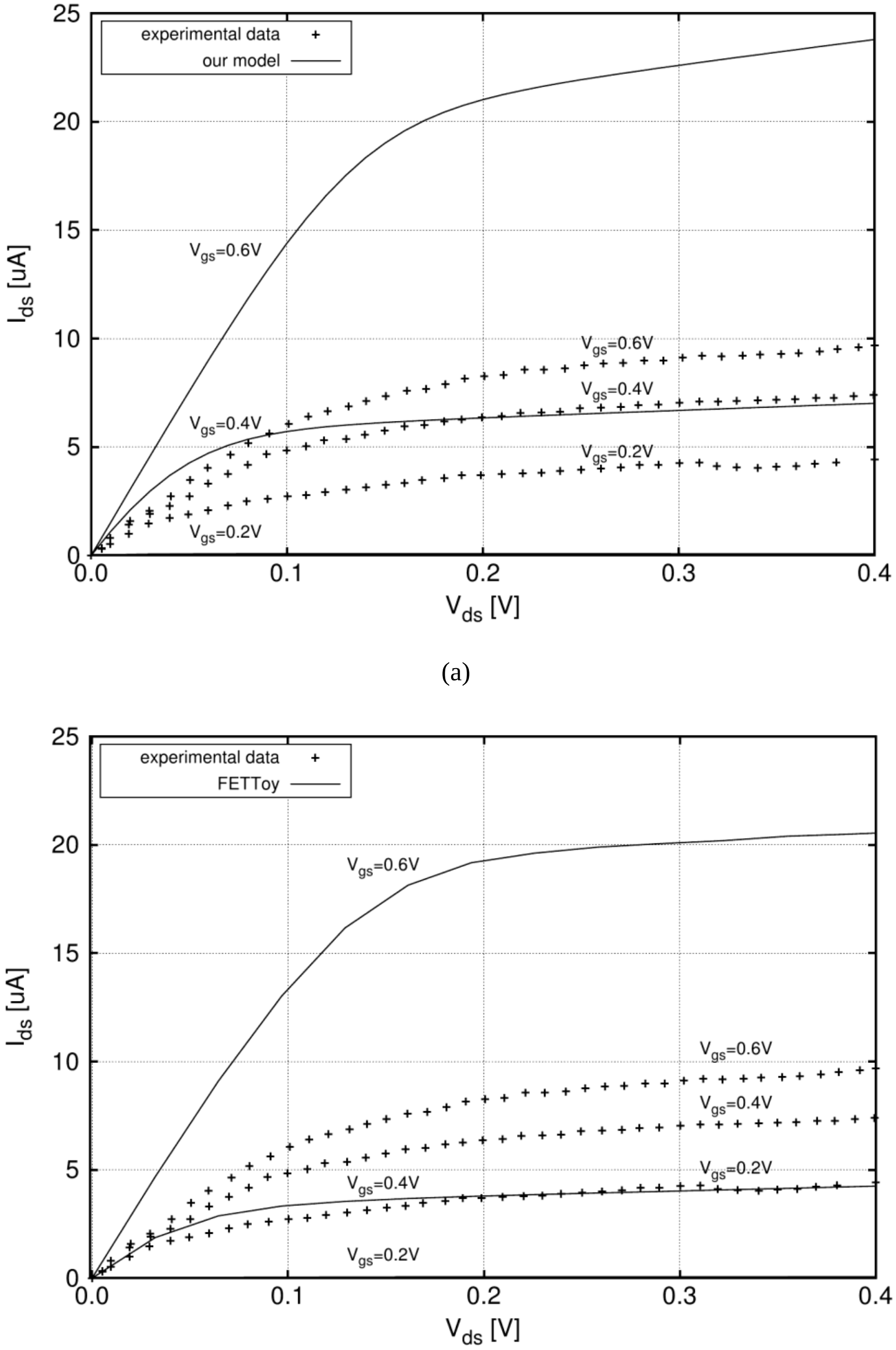


(b)

Figure 2. I_{DS} versus V_{GS} at different temperatures and different V_{DS} for: proposed model (a); FETToy model (b).

As it is possible to observe from Fig. 2, at V_{DS} = 0.8 V the current raises, when temperature decreases from 500 K to 250 K, while the threshold voltage of the device decreases. Moreover, for V_{DS} > 0.8 V. both in our model and in FETToy model the current dependence on temperature is almost zero. While the current rises with temperature T is present also at V_{DS} = 0.05 V for V_{GS} < 0.4 V, the dependence is inverted for our and FETToy models for V_{GS} > 0.4 V.

Moreover, in order to validate the obtained data, we have compared the considered models at 300 K with experimental data [18], as shown in Fig. 3.



(a)

(b)

Figure 3. I_{DS} versus V_{DS} at 300 K and different V_{GS} for: proposed model (a); FETToy model (b), in comparison with experimental data (dots).

From Fig. 3 we observe that there is a low agreement between experimental values (dots) and those simulated (line) for the considered models, since, to have low computational cost, they do not consider both ballistic and non-ballistic transport effects [18].
The simulation results, at 250 K and 500 K, are summarized in Table 1.

Table 1. Values of I_{DS} vs V_{DS} at different temperatures for: proposed model (a); FETToy model (b).

V_{GS}	**Knee Region**		**Saturation Region** (at V_{DS} = 0.8 V)	
	250 K	500 K	250 K	500 K
0.2 V	V_{DS} = 0.027 V I_{DS} = 9.41 nA	V_{DS} = 0.054 V I_{DS} = 288 nA	I_{DS} = 10.5 nA	I_{DS} = 0.365 µA
0.4 V	V_{DS} = 0.043 V I_{DS} = 3.03 µA	V_{DS} = 0.079 V I_{DS} = 4.73 µA	I_{DS} = 5.64 µA	I_{DS} = 7.56 µA
0.6 V	V_{DS} = 0.123 V I_{DS} = 16.3 µA	V_{DS} = 0.146 V I_{DS} = 16.0 µA	I_{DS} = 25.2 µA	I_{DS} = 25.4 µA
0.8 V	V_{DS} = 0.238 V I_{DS} = 30.9 µA	V_{DS} = 0.223 V I_{DS} = 32.0 µA	I_{DS} = 44.1 µA	I_{DS} = 44.1 µA

(a)

V_{GS}	**Knee Region**		**Saturation Region** (at V_{DS} = 0.8 V)	
	250 K	500 K	250 K	500 K
0.2 V	V_{DS} = 0.037 V I_{DS} = 3.6 nA	V_{DS} = 0.059 V I_{DS} = 174 nA	I_{DS} = 154 nA	I_{DS} = 0.416 µA
0.4 V	V_{DS} = 0.051 V I_{DS} = 2.49 µA	V_{DS} = 0.090 V I_{DS} = 3.96 µA	I_{DS} = 4.84 µA	I_{DS} = 6.66 µA
0.6 V	V_{DS} = 0.136 V I_{DS} = 17.2 µA	V_{DS} = 0.166 V I_{DS} = 17.0 µA	I_{DS} = 22.0 µA	I_{DS} = 22.5 µA
0.8 V	V_{DS} = 0.261 V I_{DS} = 37.1 µA	V_{DS} = 0.277 V I_{DS} = 35.6 µA	I_{DS} = 42.2 µA	I_{DS} = 42.3 µA

(b)

In particular we have reported V_{DS} and I_{DS} values in the knee region at different temperature and for different V_{GS}. The values of the threshold current are shown in the right part of the Table 1 for the two considered temperatures (250 K and 500 K) and for different gate-source voltages.

From Table 1**,** it is possible to notice easily that when V_{GS} increases, the saturation voltage ($V_{DS, SAT}$) increases. This consideration is valid for the considered models and occurs for the considered temperatures during the simulations.

Moreover the results show that the values of saturation current for different temperature are equal for high V_{GS} for the proposed model and the FETToy numeric model.

In Table 2**,** we have reported the results extracted from trans-characteristics of Fig. 2.

Table 2. Results extracted from trans-characteristics simulations.

	Our Model		**FETToy Model**	
V_{DS}	Threshold Voltage		Threshold Voltage	
	250 K	500 K	250 K	500 K
0.05 V	V_{GS} = 0.33 V	V_{GS} = 0.26 V	V_{GS} = 0.34 V	V_{GS} = 0.29 V
0.8 V	V_{GS} = 0.34 V	V_{GS} = 0.33 V	V_{GS} = 0.38 V	V_{GS} = 0.37 V

In particular it is possible to evaluate the threshold voltage of the device at temperatures of 500 K and 250 K with V_{DS} equal to 0.8 V and 0.05 V.

Moreover, we underline how for different temperatures and different V_{GS} threshold voltages for both models are nearly coincident.

All simulations were carried out in ADS 2014 on an Asus K55VD computer which uses an Intel Core i-7 3630QM processor running at 2.4 GHz, with 4 GB of RAM memory. Moreover we have obtained almost a similarity in execution times of the simulations but our model for all simulations presents a run time less than that of FETToy model.

4. CONCLUSIONS AND FUTURE DEVELOPMENTS

In this paper, we have presented a comparison of temperature dependence of I-V characteristics in CNTFETs models proposed in the literature in order to identify the one more easily implementable in simulation software for electronic circuit design.

In particular we have compared our DC CNTFET model with the online numerical model FETToy, analyzing their behaviour with changing temperature.

We have compared the two models at 300 K with experimental data, obtaining a low agreement between for all considered models, since, in order to have low computational cost, they do not consider both ballistic and non-ballistic transport effects.

Then, for any model, in order to study the effects of temperature on I-V characteristics, we have considered the temperature variation in the formula of current I_{DS}.

We have shown how the results obtained for different temperatures (250 K and 500 K) are consistent with the two considered models, because the obtained I-V characteristics are comparable.

However, our model presented a shorter run time, without losing accuracy.

Actually we are also investigating about the effect of temperature [19-21] and of noise [22] in the CNTFET-based design of analog and digital circuits.

Moreover we are studying the effects of parasitic elements of interconnection lines in CNT embedded integrated circuits [23] and the impact of technology on CNTFET-based circuits performance [24].

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